AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Original) A structure of single-poly EPROM which is suitable for using as memory cell in a substrate, comprising:

an isolation region disposed in the substrate to define a striped active area;

a deep well of first conductive type located under the isolation region and the striped active area;

a gate oxide layer disposed on the striped active area on the substrate;

a pair of selective gates disposed on the gate oxide layer and the isolation region, wherein the pair of selective gates are striped and perpendicular to the striped active area;

a pair of floating gates disposed on the gate oxide layer, and are corresponding to the active area, wherein a gap is formed between the pair of floating gates and the pair of selective gates;

a well of second conductive type disposed in the deep well of first conductive type below the pair of selective gates and the pair of floating gates;

a pair of sources disposed on both sides of the well of second conductive type, the pair of sources connected to each other via the deep well of first conductive type; and

a drain disposed in the well of second conductive type between the pair of selective gates.

9. (Original) The structure of claim 8, wherein the isolation region is a field oxide layer.

10. (Original) The structure of claim 8, wherein the isolation region is a shallow trench isolation.

11. (Original) The structure of claim 8, wherein the pair of floating gates and the pair of selective gates are polysilicon.

12. (Original) The structure of claim 8, wherein the pair of sources are laterally extended to half the width of the pair of floating gates.

13. (Canceled)

14. (Canceled)